DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Response to Amendment

The Amendment, filed on July 30, 2008 has been entered and acknowledged by the Examiner.
Claims 6-13 are pending in the instant application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-11 are rejected under 35 U.S.C. 103 (a) as being unpatentable under Park et al (US PG Pub. No. 2004/0004443) in view of Yamazaki et al (US Patent No. 6,847,050).

Regarding Claim 6, Park discloses a subpixel (Paragraph [0031], line 8 (cell)) forming a pixel (8) of a color display screen (Para. [0012] lines 6-8), comprising: one display portion (cell) ; and a plurality of thin film transistors for driving the display portion (Paragraph [0031], lines 9-15, (first, second),

Park fails to disclose wherein the plurality of thin film transistors are arranged such that their channels are positioned in parallel to each another .

Yamazaki teaches, at least in Figures 3B and 4, a plurality of thin film transistors (116, 115) is one and (117, unmarked) is the other. Figure 3B shows that they are positioned in parallel to each other (drain 117 on one connected to source 116 of the other, the grain boundaries (110) are parallel and their channels are parallel) to produce a transistor capable of high-speed operation, with high current drive capability and little variation in pluralities of elements (Column 16, lines 48-54).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the parallel channel structure, as taught by Yamazaki, in the transistors of Park, to produce a transistor capable of high-speed operation, with high current drive capability and little variation in pluralities of elements.

Regarding Claim 7, Park fails to exemplify the subpixel wherein provided that a length of one side of the subpixel is 1, a channel width of at least one of the plurality of thin film transistors is 0.4 or more.

Park discloses the claimed invention except for wherein provided that a length of one side of the subpixel is 1, a channel width of at least one of the plurality of thin film transistors is 0.4 or more.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a length of one side of the subpixel as 1, and a channel width of at least one of the plurality of thin film transistors of 0.4 or more, since it has been held that where the general conditions of a claim are disclosed in the prior art,

discovering the optimum or workable range involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding Claims 8 and 9, Park discloses wherein the thin film transistors are organic thin film transistors or amorphous Si thin film transistors.(Paragraph [0040], lines 1-3 (amorphous)).

Regarding Claims 10 and 11, Park discloses wherein the display portion is an organic electroluminescence(EL) element. (Paragraph [0031], lines 3-4).

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Yamazaki (050) and Kuwabara et al (US PG Pub. No. 2003/0141504) and further in view of Veres et al (US PG Pub. NO. 2006/0105492) .

Regarding Claims 12 and 13, Park, as modified by Yamazaki, fails to exemplify the subpixel wherein the channels of the plurality of thin film transistors are subjected to a rubbing process.

Kuwabara teaches in Paragraph [0234], lines 1-4, subjecting the active matrix substrate which includes the TFT's (line 1) to a rubbing process.

Furthermore, Veres teaches that the rubbing process is used to induce the orientation of the organic semiconductor in order to enhance carrier mobility.(Paragraph [0055], last four lines).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the rubbing process as taught by Kuwabara into the TFT

channel of Park, as modified by Yamazaki and Veres, to induce the orientation of the organic semiconductor in order to enhance carrier mobility.

Response to Arguments

Applicant's arguments with respect to claim 1 has been considered but is moot in view of the new ground(s) of rejection. The addition of the limitation requiring the channels of the transistors to be positioned in parallel to each other requires a new search and new prior art.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DONALD L. RALEIGH whose telephone number is (571)270-3407. The examiner can normally be reached on Monday-Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel can be reached on 571-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Peter J Macchiarolo/
Primary Examiner, Art Unit 2879

/Donald L Raleigh/
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